APPARATUS AND METHOD FOR GENERATING A DELAYED CLOCK SIGNAL

ABSTRACT OF THE DISCLOSURE

An apparatus and method for generating a delayed clock signal is provided. The clock signal generator includes a synchronizing circuit for generating an output clock signal from an input clock signal and further includes a delay circuit having an input coupled to the output of the synchronizing circuit. The delay circuit provides an output clock signal having a delay with respect to the clock signal from the synchronizing circuit according to one of a plurality of programmable time delays selected in accordance with a selection signal. The method of generating a clock signal includes synchronizing an internal clock signal to an external clock signal, and delaying the internal clock signal different amounts based on a selection value indicative of external clock frequency to provide the clock signal.